Packaging of silicon photodiodes for use as cryogenic electrical substitution radiometer

Eivind Bardalen[1], Marit Ulset Nordsveen[2], Per Ohlckers[1], and Jarle Gran[2]

[1] *University of South-Eastern Norway, Borre, Norway,* [2] *Justervesenet, Kjeller, Norway,*
Corresponding e-mail address: eba@usn.no

A technique for packaging photodiodes for use as a cryogenic electrical substitution radiometer was developed. Thermal simulations were used to design a diffusive thermal link between the photodiode and temperature sensor to ensure equivalence between optical and electrical heating. Tests showed good agreement between the measured and simulated time constant for an assembled module supporting the model accuracy.

INTRODUCTION

The EMPIR research project chipS·CALe aims to develop new experimental techniques for optical power measurements using self-calibrating photodiodes [1]. The dual mode detector (DMD) can be operated both as a predictable quantum efficient detector (PQED) and as an electrical substitution radiometer (ESR). In PQED mode, the optical power is measured directly from the photocurrent, while in ESR mode, a temperature sensor is used to compare optical and electrical heating of the photodiode. The term self-calibrating refers to the fact that the internal losses can be determined by use of the formula:

$$\delta(\lambda) = 1 - \frac{i_{photo}}{\Phi_T} \cdot \frac{hc}{e\lambda}, \qquad (1)$$

where Φ_T is the optical power measured in ESR mode and i_{photo} is the measured photocurrent.

A proper design of the photodiode packaging is required to ensure thermal equivalence between optical and electrical heating in ESR mode. Furthermore, the module was designed using COMSOL Multiphysics simulations to give a high signal, while having low time constant.

DESIGN AND MODELLING

A silicon photodiode (PD) with size 11 mm x 11 mm x 0.5 mm functions as both the optical absorber and heater. In optical heating mode, the power is absorbed in the central part of the active layer of the photodiode, while in electrical heating mode, the power is dissipated near the topside cathode ring by applying a forward bias to the photodiode.

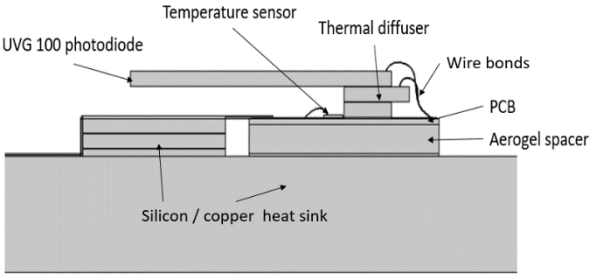

Figure 1: Sketch of DMD-detector

A thin (<200 μm) PCB with 18 μm thick copper tracks is used for electrical connections to the photodiode and temperature sensor via wire bonds and soldered wires. The temperature sensor is bonded with epoxy and wire bonded to the PCB, which is thermally coupled to the photodiode with a thermal diffuser element, consisting of a layered silicon/epoxy structure. The PCB is bonded on a thermally insulating aerogel spacer, which in turn is bonded on a machined copper heat sink. Copper wires are soldered to the edge of the PCB, forming the electrical connections to the external circuitry. These wires also form the main thermal link to the heat sink.

COMSOL's heat transfer module was used to simulate the temperature distribution in the module. The heating of the photodiode was modelled as a constant heat source, *P*. In the optical mode, the heat source was applied in an elliptical shape in the center of the photodiode, while in electrical heating mode, the heating was applied near the edges of the photodiode. The effect of the different temperature distributions in the photodiode at these different modes (T_{opt}, T_{el}) is evaluated in the photodiode in terms of inequivalence (in ppm), defined as

$$\delta_T = \frac{T_{opt} - T_{el}}{T_{opt}} \cdot 10^6 \qquad (2)$$

Simulation results show inequivalence in the temperature sensor below 1 ppm at temperatures 80 K and 35 K, and higher than 100 ppm at 300 K. At 300 K, the grey-body thermal emission from hotspots lead to the higher inequivalence. As shown in Figure 2, the inequivalence is reduced from more than 1000 ppm in the photodiode to less than 1 ppm in the temperature sensor. This is likely due to the low

thermal conductance (k) of the epoxy, which in combination with the high thermally conducting silicon lead to an effectively anisotropic thermal conductance, where $k_z < k_{x,y}$.

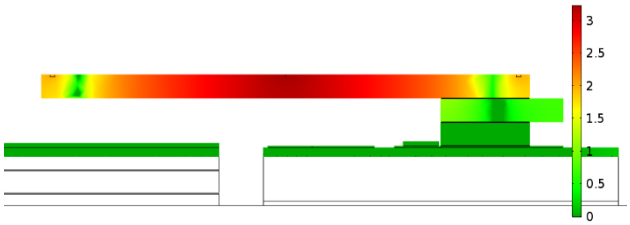

Figure 1: Logarithm of inequivalence at 80 K ($\log(\delta_T)$)

The RC time constant of the system is largely decided by the heat capacity, C_{PD}, of the photodiode and the thermal resistance of the weak link, R. In the ideal case:

$$\tau = R \cdot C_{PD} \qquad (3)$$

Since the temperature increase ΔT for an input power P is given by $\Delta T = R \cdot P$, the thermal resistance also takes the meaning of responsivity: $R = \Delta T / P$.

The simulation results, as shown in Figure 4, give a time constant that is around 50% higher than given by eq. (3). This is likely caused by the additional thermal capacitances in the system, such as that of the thermal diffuser, adhesive layers and PCB.

FABRICATION AND TESTS

An assembled module, as shown in Figure 3, was tested in vacuum at 285 K, 80 K and 35 K. Time constant measurements were performed by heating the module both optically and electrically, with cooldown to base temperature between each heating step. The 1/e time constant was then found from an exponential fit of the temperature signal. Electrical heating was done by applying a forward bias voltage to the photodiode, while optical heating was done by a 594 nm laser beam hitting the centre active area of the photodiode, while having an open electrical circuit. In both cases, the heating power was 270 µW.

Table 1 shows the measured and simulated time constant for the device at three temperatures. At 285 K and 80 K, the experimental values agree fairly good, while at 35 K the time constant is significantly higher than the simulated one. The overall good agreement between measured and simulated values supports the accuracy of the model, but more accurate material data is required for low temperatures.

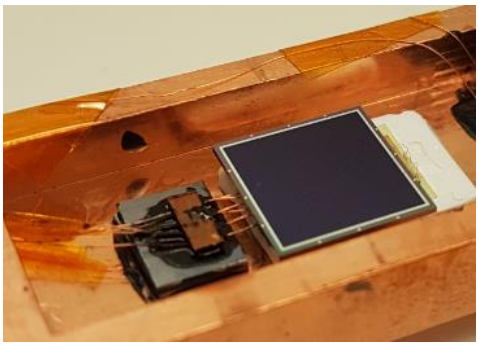

Figure 3: Assembled DMD-module

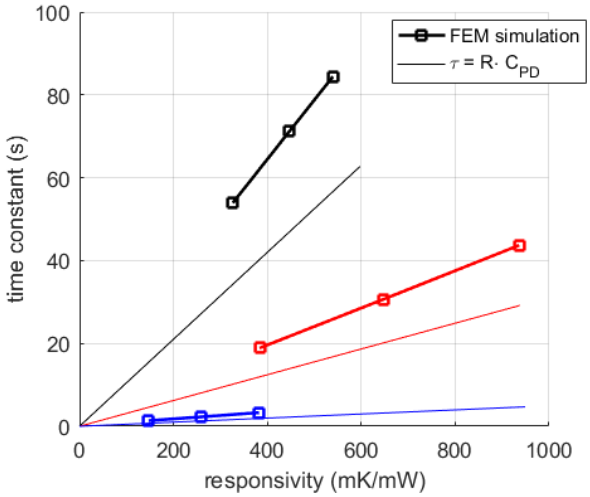

Figure 4: Simulated time constant vs. responsivity at 300 K (black), 80 K (red) and 35 K (blue). Solid lines show theoretical limit given by eq. (2)

Table 1: Experimental and simulated time constant for assembled module.

Temperature	τ (s) (experimental)	τ (s) (simulated)
285 K	83.5	81.2
80 K	41.8	36.8
35 K	10.3	2.8

ACKNOWLEDGEMENT

This project has received funding from the EMPIR programme co-financed by the Participating States and from the European Union's Horizon 2020 research and innovation programme.

REFERENCES

1. Jarle Gran. (2019, June 26). Publishable Summary for 18SIB10 chipS·CALe. Zenodo. http://doi.org/10.5281/zenodo.3545677